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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,656	07/28/2003	Phillip Johnson	1054.022	4429

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MENDELSOHN AND ASSOCIATES PC
1515 MARKET STREET
SUITE 715
PHILADELPHIA, PA 19102

EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,656	JOHNSON ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21* is/are allowed.

6)☒ Claim(s) *1,2,9-11 and 19* is/are rejected.

7)☒ Claim(s) *3-8, 12-18, 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-28-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

It is noted that applicant has not completed the cite of the 2001 Foley reference in the submitted 1449 form. The examiner has completed this cite but request that applicant check the enclosed 1449 form for accuracy.

Claim Objections

Claims 3-7 and 12-18 are objected to because of the following informalities: Claims 3 and 12 refers to "the user-programmable accuracy level" yet only a "programmable accuracy level" is set forth to provide proper support for this phase in claims 3 and 12. It is clearly apparent what applicant meant and that this is a mere typo. Thus for examining purposes claims 3 and 12, and those claims that depend on claims 3 and 12 are read as if applicant further limited "the programmable accuracy" of the independent claims to one that is user-programmable in the dependent claims. Note that the above noted claims that depend upon claim 3 contain the above issue because of their dependency on claim 3 and above noted claims that depend upon claim 12 contain the above issue because of their dependency on claim 12. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9 and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Foley et al. CMOS DLL based 2v, 3.2ps Jitter, 1Ghz Clock Synthesizer and Temperature-Compensated Tunable Oscillator" IEEE Journal of Solid State Circuits vol. 36, Issue 3 March 2001 of record (Foley 2001).

Figure 3-5 and the relevant text of Foley disclose a method for monitoring the operation of a "multiphase clock generator", i.e. delay locked loop (dll) and the associated device for doing so. The lock decode circuitry determines whether the operation of the dll has settled to a stable operating point "within a programmable accuracy level" and determines whether the stable operating point corresponds to a proper lock state for the dll. The sensing of the multiple phased clock signals at the rising edge of the reference clock determines if the dll is locked and whether it is proper locked state. Note that applicant has not set forth any specific definition for the term "programmable" or the phase "programmable accuracy level". Thus a fair and reasonable interpretation of these terms would be that the lock decode circuitry of Foley determines whether the dll has settled to a stable operating state "within a programmable accuracy level" for the device of Foley has been preprogrammed via the selection of the

various logic elements and this programmable accuracy level appears to be within one "T" as referred to by applicant. This is giving the claimed invention the broadest reasonable interpretation consistent with the supporting description (See MPEP 2111 and 904.01). Note that the lock decode circuitry of Foley is "adapted to" i.e. it is capable of determining whether the operation of the dll has settled to a stable operating point "within a programmable accuracy level" and whether the stable operating point corresponds to a proper lock state for the dll as noted above. It has been long held that "adapted to" is not a positive limitation (See MPEP 2106). Also note that the over and under signals provide for correction and since the device of Foley had to be programmed prior to its use as noted above, the lock and detection and correction circuitry of Foley is programmable. It clearly was programmed to provide a predetermined accuracy level.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 9-11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over von Kaenel 6,504,408 (Kaenel) in view of Foley et al. CMOS DLL based 2v, 3.2ps Jitter, 1Ghz Clock Synthesizer and Temperature-Compensated Tunable Oscillator" IEEE Journal of Solid State Circuits vol. 36, Issue 3 March 2001 of record (Foley 2001) and Greenfield et al. "Using Mircoprocessors and Microcomputers" The 6800 Family (Greenfield).

Figure 1 and the relevant text of Kaenel disclose a dll (delay locked loop) that can perform the functions of "clock generator" or multiphase clock generator, and Kaenel also discloses a method of monitoring the operation of the clock. The invention of Kaenel includes a phase detector 12 that in combination with the counter 14 also performs a determining operation that determines whether the device of Kaenel has locked, i.e. has "settled to a stable operating point to within a programmable accuracy level". As noted above, applicant has not set forth any specific definition for the term "programmable" or the phase "programmable accuracy level". Thus a fair and reasonable interpretation of the these terms would be that the internal circuit of Kaenel determines whether the dll has settled to a stable operating state "within a programmable accuracy level" for the device of Kaenel has been

preprogrammed via the selection of the specifics of the internal circuit to the phase comparator and the selection of the maximum count of the counter 14. Note that just like that disclosed by applicant the selection of the maximum count determines the how many values of "T" the dll can be off and thus this is a accuracy level that is programmable by the selection of the maximum count. Note that Kaenel does not limit the count to only one value. Kaenel also includes a digital delay line 16 that applicant sometimes refers to as a "clock-generation circuitry". Because it is a delay line as shown in Figure 4, it has the capability of generating a plurality of clock signals having different relative phases based on a count value received from the counter. Again note that applicant has used the term "adapted to" which has been held to not set forth a positive limitation (See MPEP 2106). Thus the claimed invention does not require that the "adapted to" be preformed just that the prior art has to be capable of performing the recited function in order to meet the claim(s). The values from the phase/lock detector is digital and note that these values are accumulated i.e. gathered by the counter via the counter control circuit. Note that the phase/ lock detector of Kaenel is not only adapted to but actually does compare the reference clock to a feedback signal obtained from the "Output clock" signal as is clearly illustrated. The output of Kaenel is based on this comparison. Kaenel appears to lack circuitry to determine whether or not a proper lock has been obtained. Accordingly, it does not appear that Kaenel is capable of determining whether or not a proper lock has been obtained.

Foley discloses a logic circuit that is programmed to determine how the phase shifted signals of the "clock generation circuit" compare to each other at a certain point of the reference clock signal. Note in particular Figure 4. This determines if the lock has been proper and if not this circuit causes the counter to change values accordingly.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided Kaenel with a similar proper lock state detector like that of Foley so as to determine whether or not the stable point of Kaenel is an actual proper lock and if not to correct this by changing the value of the counter so at to provide for a proper lock as taught by Foley.

As noted above the term "programmable" has been given its plain meaning. However, even in the case that programmable is taken to me a computer program, a very narrow interpretation of "programmable", this too would have been obvious to one of ordinary in the art at the time the invention was made. Note that Greenfield teaches the well know fact that hard-wired devices can be implemented via a microprocessor thereby allowing the program of the hard-wired device to be changed. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed any of the hard-wired devices noted above via a microprocessor because of the art recognized

equivalence of these structures. One of ordinary skill would have additionally been motivated to do so because the selected program of these hard-wired devices can be changed by the user via the computer program in the microprocessor arrangement as taught by Greenfield.

Claims 3-8, 12-18, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 21 is allowable over the art of record.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Figure 10 of Erickson 5,815,016 and Takada et al. 6,259,290 discloses a similar proper lock detector to Foley. Hirai 6,794,944 and JP 2002314409A discloses a similar lock detector that is described by applicant's specification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Mondays. The examiner normally has the second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
December 7, 2004

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817